## REMARKS

This is a full and timely response to the outstanding Action mailed September 15, 2004. Upon entry of the amendments in this response, claims 1 - 5, 7 - 13, 15 - 19 and 21 - 27 remain pending. In particular, Applicants have amended claims 1, 7 – 9, 15, 21 - 23 and 25, and have canceled claims 6, 14, 20 and 28 without prejudice, waiver, or disclaimer. Applicants have canceled claims 6, 14, 20 and 28 merely to reduce the number of disputed issues and to facilitate early allowance and issuance of other claims in the present application. Applicants reserve the right to pursue the subject matter of this canceled claim in a continuing application, if Applicants so choose, and do not intend to dedicate the canceled subject matter to the public. Reconsideration and allowance of the application and presently pending claims are respectfully requested.

**In the Drawings**

The Office Action indicates that the drawings stand objected to under 37 CFR 1.83(a), because features recited in claims 6, 14, 20 and 28 allegedly are not shown. In this regard, Applicant has canceled claims 6, 14, 20 and 28, and respectfully submits that the drawing objections have been rendered moot.

**Objections to the Claims**

The Office Action indicates that several of the claims stand objected to because of various informalities. In this regard, Applicant has corrected grammatical errors in the specification, the abstract, and the claims as set froth above. Applicant respectfully submits that no new matter has been introduced and that the claim objections have been rendered moot.

**Rejections under 35 U.S.C. 102**

The Office Action indicates that claims 1, 3, 5, 7, 15, 17, 19 and 21 stand rejected under 35 U.S.C 102(b) as being anticipated by *Liu et al* (U.S. 6,265,752). Additionally, the Office Action indicates that claims 1, 2, 5-10, 13-16, 19-24, 27 and 28 stand rejected under 35 U.S.C 102(b) as being anticipated by *Ito et al* (U.S. 5,856,695). With respect to claims 6, 14, 20 and 28, Applicant has canceled these claims and respectfully asserts that the rejection as to these claims has been rendered moot. With respect to the remaining claims, Applicant respectfully traverses the rejection.

Turning first to *Liu*, it appears that the Office Action equates the P-well and N-well disclosed by *Liu* to Applicant's "first and second wells" in claims 1 and 15. However, *Liu* discloses a HVNMOS with an N+ buried layer combined with an N well, in which a field oxide region 26 on the N well serves as the drain region, where the gate oxide 28 and the gate 30 are formed thereon (please see col. 3, lines 37-43 and FIG. 4). Moreover, *Liu* discloses that a portion of the gate 30 lies on a portion of the field oxide 26, which reduces the electric field near the drain (*Liu* at col. 3, lines 46-49). Clearly, *Liu* does not teach or suggest that there is no field oxide formed between the gate and the wells.

With respect to *Ito*, it appears that the Office Action equates element 1350 disclosed by *Ito* as Applicant's "gate" in claims 1 and 15. Additionally, it appears that the Office Action equates elements 850 and 750 disclosed by *Liu* to Applicant's "first and second wells" in claims 1 and 15. However, *Ito* discloses a BiCMOS, which includes an NMOS gate 1350 formed on the P-well 850 and an isolation oxide region 620 formed between the gate 1350 and the N-well 750 (*Ito* at FIGS. 8 and 18). Clearly, *Ito* does not teach or suggest that the gate is formed on a junction between the wells and that there is no field oxide formed between the gate and the wells.

Moreover, it appears that the Office Action equates elements 1356 and 1160 disclosed by *Ito* with Applicant's "first and second gates" in claims 9 and 23. Additionally, it appears that the Office Action equates elements 850 and 750 and the elements 770 and 860 disclosed by *Ito* with Applicant's "first P and N wells" and "second N and P wells" in claims 9 and 23. However, *Ito* discloses a BiCMOS, which includes a PMOS gate 1356 formed on the N-well 750, an NMOS gate 1160 formed on the P-well 860, an isolation oxide region 620 formed between the PMOS gate 1356 and the P-well 850, and another isolation oxide region 620 formed between the NMOS gate 1160 and the N-well 770 (*Ito* at FIGS. 8 and 18). Clearly, *Ito* does not teach or suggest that the gate is formed on a junction between the wells and that there is no field oxide formed between the gate and the wells.

Turning now to the claims, amended claim 1 recites:

> 1. A high voltage device comprising:
> a substrate of a first type;
> first and second wells respectively of the first type and a second type in the substrate;
> ***a gate formed on a junction between the first and second wells, without a field oxide between the gate and the first and second wells***;
> first and second doped regions both of the second type, respectively formed in the first and second wells and both sides of the gate; and
> a third doped region of the first type in the first well and adjacent to the first doped region.

(*Emphasis added*).

Applicant respectfully asserts that neither of the cited references teaches nor otherwise discloses at least the limitations emphasized above in claim 1. Therefore, Applicant respectfully asserts that the rejection of claim 1 is improper, and requests that claim 1 be placed in condition for allowance. Since claims 2, 3, 5, 7 and 8 are dependent claims that incorporate the limitations

of claim 1, and are not otherwise rejected, Applicant respectfully requests that these claims also be placed in condition for allowance.

With respect to amended claim 9 that claim recites:

> 9. A high voltage device formed on a P substrate comprising:
> an HVNMOS comprising:
> first P and N wells in the P substrate;
> ***a first gate formed on a junction between the first P and N wells, without a field oxide between the gate and the first P and N wells***;
> two first N+ doped regions respectively formed in the first P and N wells, and both sides of the first gate; and
> a first P+ doped region in the first P well and adjacent to the first N+ doped region in the first P well; and
> a HVPMOS comprising:
> an N+ buried layer in the P substrate;
> second N and P wells in the P substrate and above the N+ buried layer;
> ***a second gate formed on a junction between the second N and P wells, without a field oxide between the gate and the second P and N wells***;
> two second P+ doped regions respectively formed in the second N and P wells, and both sides of the second gate; and
> a second N+ doped region in the second N well and adjacent to the second P+ doped region in the second N well.

(*Emphasis added*).

Applicant respectfully asserts that neither of the cited references teaches nor otherwise discloses at least the limitations emphasized above in claim 9. Therefore, Applicant respectfully asserts that the rejection of claim 1 is improper, and requests that the rejection be removed.

With respect to amended claim 15 that claim recites:

> 15. A method for manufacturing a high voltage device, comprising the steps of:
>
> providing a substrate of a first type;
>
> forming first and second wells respectively of the first type and a second type in the substrate;
>
> ***forming a gate on a junction between the first and second wells, without a field oxide formed between the gate and the first and second wells***;
>
> forming first and second doped regions both of the second type, respectively in the first and second wells and both sides of the gate; and
>
> forming a third doped region of the first type in the first well and adjacent to the first doped region.

(*Emphasis added*).

Applicant respectfully asserts that neither of the cited references teaches nor otherwise discloses at least the limitations emphasized above in claim 15. Therefore, Applicant respectfully asserts that the rejection of claim 15 is improper, and requests that claim 15 be placed in condition for allowance. Since claims 16, 19, 21 and 22 are dependent claims that incorporate the limitations of claim 15, and are not otherwise rejected, Applicant respectfully requests that these claims also be placed in condition for allowance.

With respect to amended claim 23 that claim recites:

> 23. A method for manufacturing a high voltage device comprising the steps of:
>
> providing a P substrate;
>
> forming a HVNMOS on the P substrate by:
>
> forming first P and N wells in the P substrate;
>
> ***forming a first gate on a junction between the first P and N wells, without a field oxide between the gate and the first P and N wells***;
>
> forming two first N+ doped regions respectively in the first P and N wells, and both sides of the first gate; and
>
> forming a first P+ doped region in the first P well and adjacent to the first N+ doped region in the first P well; and
>
> forming a HVPMOS on the P substrate by:

forming an N+ buried layer in the P substrate;
forming second N and P wells in the P substrate and above the N+ buried layer;
***forming a second gate on a junction between the second N and P wells, without a field oxide between the gate and the second P and N wells***;
forming two second P+ doped regions respectively in the second N and P wells, and both sides of the second gate; and
forming a second N+ doped region in the second N well and adjacent to the second P+ doped region in the second N well.

(*Emphasis added*).

Applicant respectfully asserts that neither of the cited references teaches nor otherwise discloses at least the limitations emphasized above in claim 23. Therefore, Applicant respectfully asserts that the rejection of claim 23 is improper, and requests that claim 23 be placed in condition for allowance. Since claim 24 is a dependent claim that incorporates the limitations of claim 23, and is not otherwise rejected, Applicant respectfully requests that this claim also be placed in condition for allowance.

Applicant respectfully asserts that support for the aforementioned amendments can be found at FIG. 4 of the present application, for example, wherein the gate 422 is formed on a junction of the P and N wells 411 and 412, without any field oxides between the gate 422 and the P and N wells 411 and 412. Additionally, at FIG. 6F, the gates 662 are respectively formed on a junction of the P and N wells 631 and 632 and a junction of the P and N wells 642 and 641, without any field oxides between the gate 422 and the P and N wells 631 and 632 or the gate 422 and the P and N wells 642 and 641.

**Rejections under 35 U.S.C 103**

The Office Action indicates that claims 9, 11, 13, 23, 25, and 27 stand rejected under 35 U.S.C 103(a) as being unpatentable over *Liu* in view of *Wei et al.* (U.S. 6,403,992). Additionally, the Office Action indicates that claims 3, 4, 11, 12, 17, 18, 25 and 26 stand rejected under 35 U.S.C 103(a) as being unpatentable over *Ito* in view of *McElheny et al.* (U.S. 6,740,944). Applicant respectfully traverses the rejections.

As set forth above, Applicant respectfully asserts that *Liu* and *Ito* do not teach or reasonably suggest at least certain limitations that have been emphasized in the respective independent claims. Since *Wei* and *McElheny* also do not teach or reasonably suggest at least these limitations, Applicant respectfully asserts that the rejection of claims 3, 4, 9, 11 - 13, 17, 18, 23 and 25 – 27 is improper and that these dependent claims are in condition for allowance.

**Cited Art Made of Record**

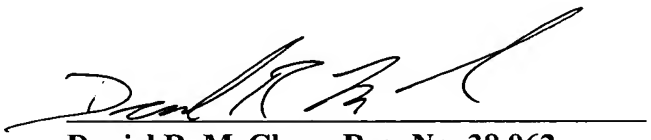
The cited art made of record has been considered, but is not believed to affect the patentability of the presently pending claims.

## CONCLUSION

In light of the foregoing amendments and for at least the reasons set forth above, Applicant respectfully submits that all objections and/or rejections have been traversed, rendered moot, and/or accommodated, and that the now pending claims are in condition for allowance. Favorable reconsideration and allowance of the present application and all pending claims are hereby courteously requested. If, in the opinion of the Examiner, a telephonic conference would expedite the examination of this matter, the Examiner is invited to call the undersigned attorney at (770) 933-9500.

No fee is believed to be due in connection with this amendment and response to Office Action. If, however, any fee is believed to be due, you are hereby authorized to charge any such fee to deposit account No. 20-0778.

Respectfully submitted,



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